Listing of the Claims:

1. (Previously Amended) A semiconductor capacitor having a lower electrode, a dielectric layer and an upper electrode, wherein the upper electrode comprises a deposition structure including three layers including a doped polysilicon layer formed between a first undoped polysilicon layer and a second undoped polysilicon layer, and a first metal pattern formed deposited over the upper electrode, wherein the semiconductor capacitor is a wire-bond attached chip capacitor.

2. (Original) The capacitor, as defined in claim 1, wherein the first and second undoped polysilicon layers are formed at a thickness of less than 1000A.

3. (Original) The capacitor, as defined in claim 1, wherein the doped polysilicon layer is formed at a thickness between 1800A and 2500A.

4. (Canceled)

5. (Original) The capacitor, as defined in claim 4, wherein the metal pattern is constructed in a deposition structure including a blocking metal layer and an aluminum layer.

6. (Original) The capacitor, as defined in claim 5, wherein the blocking metal layer is constructed in a structure including a Ti layer and a TiN layer.